In the Claims

Please cancel Claims 1-4 without prejudice.

Claims 1-22 (Cancelled)

Please add the following new Claim 23.

23. (New) A manufacturing method of a semiconductor device, in which a resistive impurity layer formed in an active region, and an insulation gate type heavy insulated transistor and an insulation gate type light insulated transistor having different drain-source breakdown voltages, are integrated on a same semiconductor layer, comprising:

(a) forming an element isolation region and an active region, electrically isolated by the element isolation region, on the semiconductor layer;

(b) forming an insulation layer above the semiconductor layer;

(c) forming a resistive impurity layer, at least, in a part of the active region by forming a first impurity-doping region;

(d) forming a gate insulation layer of the heavy insulated transistor in a forming region for the heavy insulated transistor by patterning the insulation layer to a predetermined shape, and removing the insulation layer in forming regions for the light insulated transistor and the resistive impurity layer;

(e) forming a gate insulation layer of the light insulated transistor in the forming region for the light insulated transistor;

(f) forming a gate conductive layer of the each transistor on the first gate insulation layer and the second gate insulation layer; and

(g) forming a source/drain region of the each transistor by doping a second impurity, as well as forming a contact impurity layer in a region, continuously connected to the resistive impurity layer, and providing a second impurity-doping forbidden region, at least, in the element isolation region at the same time, while

providing a second impurity-doping region, at least in the active region in the forming region for the resistive impurity layer, and a second impurity-doping forbidden region, at least in the element isolation region,

wherein a plurality of the contact impurity layers are formed, and the second impurity-doping forbidden region is formed so as to isolate, at least the adjacent second impurity-doping regions,

wherein the element isolation region is semi-recessed LOCOS and a thickness of a gate insulation layer of said heavy insulated transistor is thicker than a gate insulation layer of said light insulated transistor.